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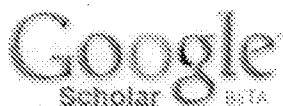
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L1	33	703/14.ccls. and @pd>"20071101"	US-PGPUB	OR	OFF	2008/04/07 12:30
L2	1307	cache same test\$3 and @ad<"20040301"	US-PGPUB	OR	OFF	2008/04/07 12:40
L3	69	cache near test\$3 and @ad<"20040301"	US-PGPUB	OR	OFF	2008/04/07 12:40
L4	43	cache near test\$3 and random and @ad<"20040301"	US-PGPUB	OR	OFF	2008/04/07 12:40
L5	73	(cache same test\$3 same random) and @ad<"20040301"	US-PGPUB	OR	OFF	2008/04/07 12:50
L6	64	L5 NOT L4	US-PGPUB	OR	OFF	2008/04/07 12:50
L7	10	((cache near design) same test\$3) and @ad<"20040301"	US-PGPUB	OR	OFF	2008/04/07 12:57

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L10	0	((cache near design) same verif\$7) and random	US-PGPUB	OR	OFF	2008/04/07 14:00

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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L12	56	(cache and sequential\$2 and random\$2 and function\$1).clm.	US-PGPUB	OR	OFF	2008/04/07 14:27
L14	14	(cache and buffer\$1 and random\$2 and verif\$7).clm.	US-PGPUB	OR	OFF	2008/04/07 14:35


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Protocol verification as a hardware design aid - all 14 versions »

 DL Dill, AJ Drexler, AJ Hu, CH Yang - Computer Design: VLSI in Computers and Processors, 1992. ... , 1992 - [ieeexplore.ieee.org](#)

 ... more bugs in the original **design** are uncovered ... The **verification** process then enters a tight loop ... 3.1 **Cache** coherence protocol Directory-based **cache** coherence is ...

 Cited by 345 - [Related Articles](#) - [Web Search](#)
Computer architecture: a quantitative approach

 DA Patterson, JL Hennessy - 1990 - [portal.acm.org](#)

 ... Mark B. Reinhold, **Cache** performance of garbage-collected programs, ACM SIGPLAN ... John

 P. Hayes, High-level test generation for **design verification** of pipelined ...

 Cited by 1507 - [Related Articles](#) - [Web Search](#) - [Library Search](#)
Automatic verification of pipelined microprocessor control - all 5 versions »

JR Burch, DL Dill - ... 6th International Conference on Computer Aided Verification, 1994 - Springer

 ... with these com- plications seems to be justified since the **cache** hit ratio is ... In G. Birtwistle, editor, Proceedings of the 1988 **Design Verification** Conference. ...

 Cited by 430 - [Related Articles](#) - [Web Search](#)
Verification of the Futurebus+ cache coherence protocol - all 7 versions »

EM Clarke, O Grumberg, H Hiraishi, S Jha, DE Long, ... - Formal Methods in System Design, 1995 - Springer

 ... Our model for the **cache** coherence protocol consists ... to reduce the complexity of **verification** (by hiding details) and to cover allowed **design** choices (indicated ...

 Cited by 239 - [Related Articles](#) - [Web Search](#) - [Library Search](#)
[book] Design and validation of computer protocols - all 12 versions »

GJ Holzmann - 1990 - Prentice-Hall, Inc. Upper Saddle River, NJ, USA

 ... RP Kurshan, Formal **verification** in a commercial ... Ganesh Gopalakrishnan, Deriving Efficient **Cache** Coherence Protocols ... Formal Methods in System Design, v.20 n.1, p ...

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[book] The directory-based cache coherence protocol for the DASH multiprocessor - all 3 versions »

D Lenoski, J Laudon, K Gharachorloo, A Gupta, J ... - 1990 - ACM Press New York, NY, USA

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Verifying a Multiprocessor Cache Controller Using Random Test Generation

- all 8 versions »

DA Wood, GA Gibson, RH Katz - IEEE Design & Test, 1990 - portal.acm.org

... The **design verification** of the **cache** controller for SPUR, a shared-memory multiprocessor, is reported. The strategy was to develop a **random** tester that would ...

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Constraint solving for test case generation: a technique for high-level design verification - all 2 versions »

AK Chandra, VS Iyengar - Computer Design: VLSI in Computers and Processors, 1992. ..., 1992 - ieeexplore.ieee.org

... **Random** test patterns have been extensively used for **design verification** of CPU pipelines, arithmetic units, controllers, **cache** memories, etc. ...

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[PDF] **Verification of the IBM RISC System 16000 by a dynamic biased pseudo-random test program generator** - all 5 versions »

E Gofman, M Leibowitz - IBM SYSTEMS JOURNAL, 1991 - research.ibm.com

... A **random** approach to automatic test generation for software and hardware **verification** ...

It was applied to the **verification** of selected **design** units such ...

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Performance optimizations, implementation, and verification of the SGI Challenge multiprocessor - all 3 versions »

M Galles, E Williams - System Sciences, 1994. Vol. I: Architecture, Proceedings of ..., 1994 - ieeexplore.ieee.org

... HDL simulation with **random**, self checking vector ... by a discussion of effective **design verification** techniques used ... UO, and may also support **cache-coherence** and ...

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... applied to validate the memory system **design** of the ... that development and validation of **cache** protocols ... greatly benefit from state-based **verification** methods. ...

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M Galles, E Williams - System Sciences, 1994. Vol. I: Architecture, Proceedings of ..., 1994 - [ieeexplore.ieee.org](#)

... by a discussion of effective **design verification** techniques used ... implements a number

of **design** features to maintain ... a complete set of duplicate **cache** tags which ...

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D Lenoski, J Laudon, K Gharachorloo, A Gupta, J ... - 1990 - ACM Press New York, NY, USA

... In order to manage the size of the prototype **design** effort, a commercial ... interfaces to a 256 Kbyte second-level write-back **cache** through a read **buffer** and a ...

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[Functional verification of a multiple-issue, out-of-order, superscalar Alpha processor-the DEC Alpha ... - all 12 versions »](#)

S Taylor, M Quinn, D Brown, N Dohm, S Hildebrandt, ... - the 35th Design Automation Conference, 1998 - [doi.ieeeecomputersociety.org](#)

... system configurations, and L2-**cache** RAM types [1 ... of timing, electrical, and physical **design** errors were ... The chip **verification** team primarily utilized simulation ...

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[Design verification of the S3. mp cache-coherent shared-memory system - all 7 versions »](#)

F Pong, M Browne, A Nowatzky, M Dubois - Computers, IEEE Transactions on, 1998 - [ieeexplore.ieee.org](#)

... applied to validate the memory system **design** of the ... that development and validation of **cache** proto- cols ... greatly benefit from state-based **verification** methods. ...

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[I'm done simulating: now what? Verification coverage analysis and correctness checking of the DECchip ... - all 2 versions »](#)

M Kantrowitz, LM Noack - Design Automation Conference Proceedings 1996, 33rd, 1996 - [ieeexplore.ieee.org](#)

... ratios, system configurations, and module-level **cache** parameters ... to estimate how much of the **design** had been ... was also an important part of the **verification** flow ...

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[RuleBase: an Industry-Oriented Formal Verification Tool - all 18 versions »](#)

I Beer, S Ben-David, C Eisner, A Landver - Design Automation Conference, 1996 - [doi.ieeeecomputersociety.org](#)

... **Verification** of the Futurebus+ **Cache** Coherence Protocol ... and K. McMillan, "Using Formal

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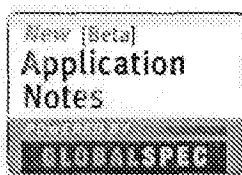
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1. **Efficient checker processor design**
Chatterjee, S.; Weaver, C.; Austin, T.;
[Microarchitecture, 2000. MICRO-33. Proceedings. 33rd Annual IEEE/ACM Int](#)
10-13 Dec. 2000 Page(s):87 - 97
Digital Object Identifier 10.1109/MICRO.2000.898061
[AbstractPlus](#) | [Full Text: PDF\(1020 KB\)](#) IEEE CNF
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2. **Multiprocessor system verification through behavioral modeling and sin**
Raghavan, R.; Kreulen, J.; O'Krafka, B.; Salamian, S.; Saha, A.; Malik, N.;
[Computers and Communications, 1995. Conference Proceedings of the 1995](#)
[International Phoenix Conference on](#)
28-31 March 1995 Page(s):396 - 402
Digital Object Identifier 10.1109/PCCC.1995.472462
[AbstractPlus](#) | [Full Text: PDF\(704 KB\)](#) IEEE CNF
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3. **Verification of an industrial CC-NUMA server**
Mukherjee, R.; Nakayama, Y.; Mima, T.;
[Design Automation Conference, 2002. Proceedings of ASP-DAC 2002. 7th As](#)
[the 15th International Conference on VLSI Design. Proceedings](#)
7-11 Jan. 2002 Page(s):747 - 752
Digital Object Identifier 10.1109/ASPDAC.2002.995023
[AbstractPlus](#) | [Full Text: PDF\(274 KB\)](#) IEEE CNF
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4. **Multiprocessor design verification for the PowerPC 620 microprocessor**
Montemayor, C.; Sullivan, M.; Jen-Tien Yen; Wilson, P.; Evers, R.;
[Computer Design: VLSI in Computers and Processors, 1995. ICCD '95. Proce](#)
[International Conference on](#)
2-4 Oct. 1995 Page(s):188 - 195
Digital Object Identifier 10.1109/ICCD.1995.528809
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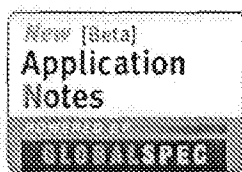
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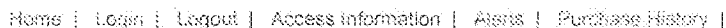
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- ☐ 1. **Verifying a multiprocessor cache controller using random test generatic**
Wood, D.A.; Gibson, G.A.; Katz, R.H.;
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Volume 7, Issue 4, Aug. 1990 Page(s):13 - 25
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[Design Automation Conference, 2000. Proceedings 2000. 37th](#)
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[AbstractPlus](#) | [Full Text: PDF\(556 KB\)](#) [IEEE CNF](#)
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Galles, M.; Williams, E.;
[System Sciences, 1994. Vol. I: Architecture, Proceedings of the Twenty-Seve](#)
[Conference on](#)
Volume 1, 4-7 Jan. 1994 Page(s):134 - 143
Digital Object Identifier 10.1109/HICSS.1994.323177
[AbstractPlus](#) | [Full Text: PDF\(788 KB\)](#) [IEEE CNF](#)
[Rights and Permissions](#)
- ☐ 4. **Alpha 21164 manufacturing test development and coverage analysis**
Stoucný, C.J.; Davies, R.; McKernan, P.; Truong, T.;
[Design & Test of Computers, IEEE](#)
Volume 15, Issue 3, July-Sept. 1998 Page(s):98 - 104
Digital Object Identifier 10.1109/54.706040
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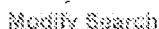
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- 1. A VLSI chip set for a multiprocessor workstation. II. A memory management controller**
Jeong, D.-K.; Wood, D.A.; Gibson, G.A.; Eggers, S.J.; Hodges, D.A.; Katz, R.H.
Solid-State Circuits, IEEE Journal of
Volume 24, Issue 6, Dec. 1989 Page(s):1699 - 1707
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- 3. The 68040 processor. 2. Memory design and chip**
Edenfield, R.W.; Gallup, M.G.; Ledbetter, W.B., Jr.; McGarity, R.C.; Quintana, J.
Micro, IEEE
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Sorin, D.J.; Plakal, M.; Condon, A.E.; Hill, M.D.; Martin, M.M.K.; Wood, D.A.;
Parallel and Distributed Systems, IEEE Transactions on
Volume 13, Issue 6, June 2002 Page(s):556 - 578
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